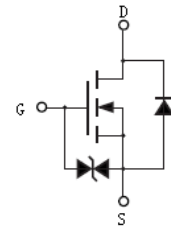


Features

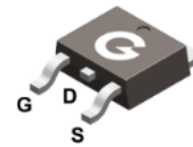
- Low power loss by high speed switching and low on-resistance
- Excellent thermal behavior
- Very low FOM for fast switching efficiency
- Product validation acc. JEDEC Standard
- Integrated ESD protection diode: HBM: JESD22-A114-B: 2
- RoHS compliant with Halogen-free

HF



Applications

- LED lighting
- Adapters
- Chargers
- Industrial power
- PFC stage



TO-252

Mechanical Data

- Case: TO-252
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte tin-plated leads; solderability-per MIL-STD-202, Method 208

Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
SJM80R1K2D	TO-252	80 pcs / Tube & 2500 pcs / Tape & Reel	SJM80R1K2D

Maximum Ratings (@ T_C = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	800	V
Gate-to-Source Voltage (Static)	V _{GSS}	±20	V
Continuous Drain Current (T _C = 25°C)	I _D	4.5	A
Continuous Drain Current (T _C = 100°C)		2.8	A
Pulsed Drain Current (t _p = 10μs, T _C = 25°C)	I _{DM}	18	A
Single Pulse Avalanche Energy ³	E _{AS}	90	mJ
Power Dissipation (T _C = 25°C)	P _D	57	W
Operating Junction Temperature Range	T _J	-55 ~ +150	°C
Storage Temperature Range	T _{STG}	-55 ~ +150	°C

Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance Junction-to-Case	R _{θJC}	-	1.9	2.2	°C/W
Thermal Resistance Junction-to-Air ¹	R _{θJA}	-	-	62	°C/W

Electrical Characteristics (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
V_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	800	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 800V, V_{GS} = 0V$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 1	μA
On Characteristics						
$R_{DS(ON)}$	Drain-Source On-resistance ^{*2}	$V_{GS} = 10V, I_D = 1.2A$	-	0.95	1.2	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3.2	4	V
R_G	Gate Resistance	$V_{GS} = 0V, f = 1MHz$	-	7.1	-	Ω
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V$	-	422	-	μF
C_{OSS}	Output Capacitance	$V_{DS} = 40V$	-	40	-	
C_{RSS}	Reverse Transfer Capacitance	$f = 250kHz$	-	1.9	-	
Switching Characteristics						
$t_{d(ON)}$	Turn-on Delay Time ^{*4}	$V_{DD} = 400V$ $I_D = 2A$ $R_G = 25\Omega$	-	19	-	ns
t_r	Turn-on Rise Time ^{*4}		-	19	-	
$t_{d(OFF)}$	Turn-Off Delay Time ^{*4}		-	58	-	
t_f	Turn-Off Fall Time ^{*4}		-	21	-	
Q_G	Total Gate-Charge	$V_{DD} = 640V$	-	16	-	nC
Q_{GS}	Gate to Source Charge	$V_{GS} = 10V$	-	4	-	
Q_{GD}	Gate to Drain (Miller) Charge	$I_D = 2A$	-	5.6	-	
Source-Drain Diode Characteristics						
V_{SD}	Diode Forward Voltage ^{*2}	$I_{SD} = 2A, V_{GS} = 0V$	-	0.83	1.3	V
t_{rr}	Reverse Recovery Time	$I_F = 2A, V_R = 400V$	-	170	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt = 100A/\mu s$	-	0.95	-	μC

Notes:

1. The data tested by surface mounted on a minimum recommended FR-4 board
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The E_{AS} data shows Max. rating. The test condition is $V_{DD} = 100V, V_{GS} = 10V, L = 50mH$
4. Guaranteed by design, not subject to production

Ratings and Characteristics Curves (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

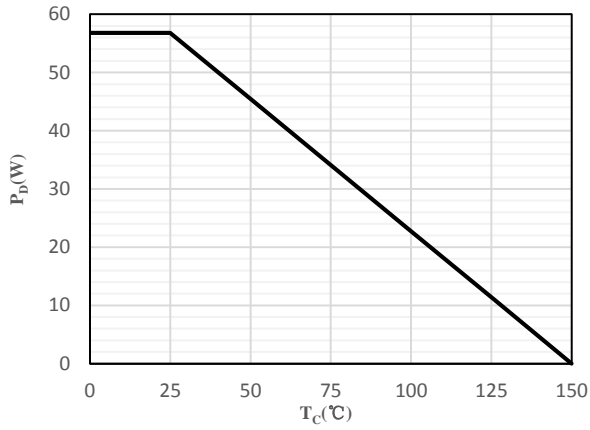


Fig 1 Power Dissipation

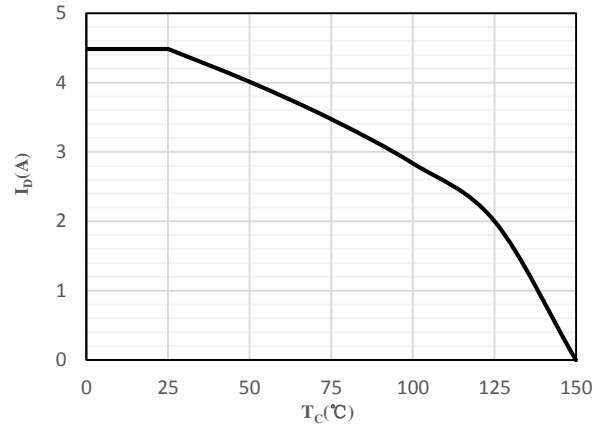


Fig 2 Drain Current

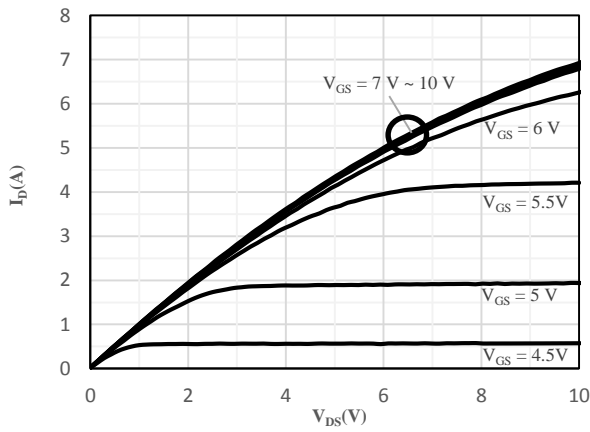


Fig 3 Typical Output Characteristics

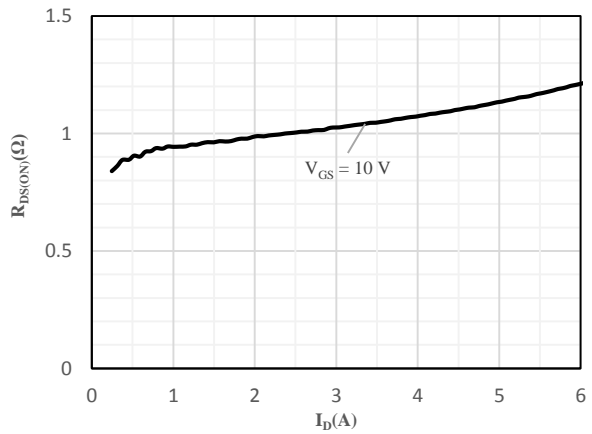


Fig 4 On-Resistance vs. Drain Current and Gate Voltage

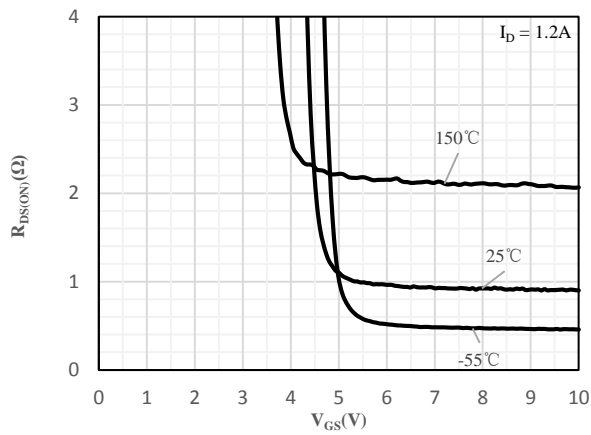


Fig 5 On-Resistance vs. Gate-Source Voltage

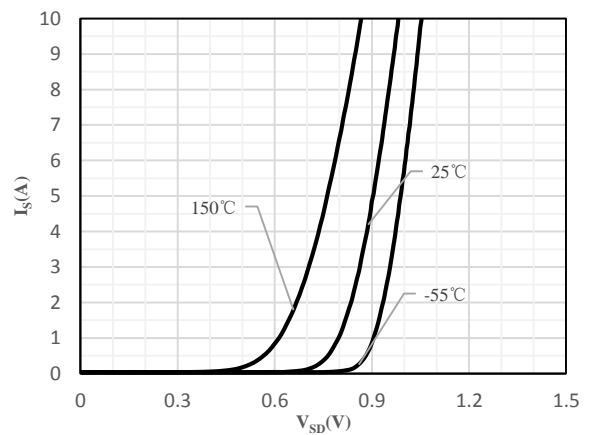


Fig 6 Body-Diode Characteristics

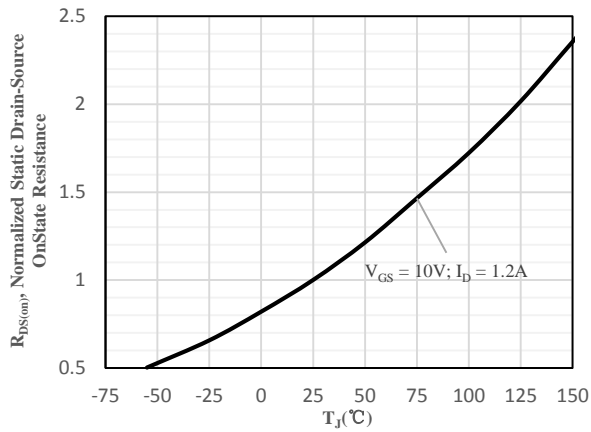


Fig 7 Normalized On-Resistance vs. Junction Temperature

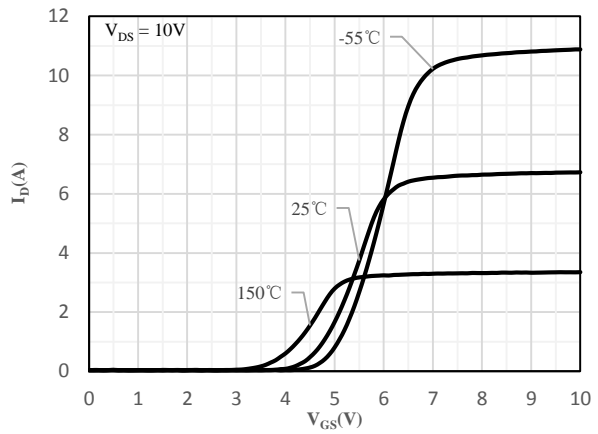


Fig 8 Transfer Characteristics

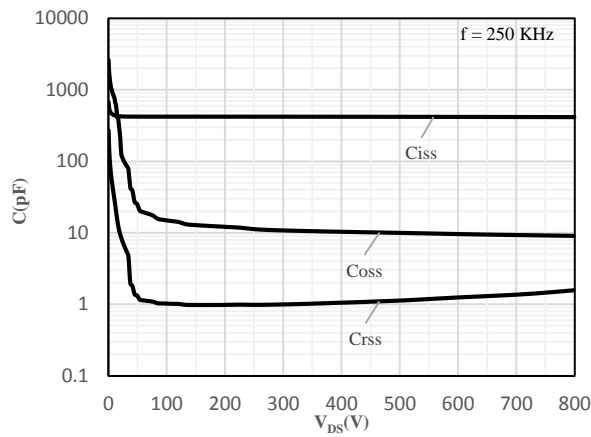


Fig 9 Capacitance Characteristics

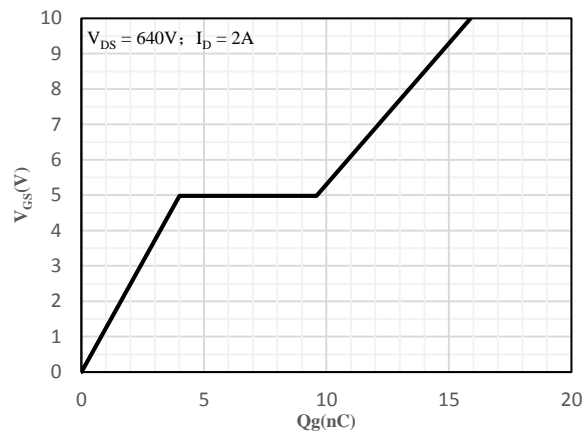


Fig 10 Gate-Charge Characteristics

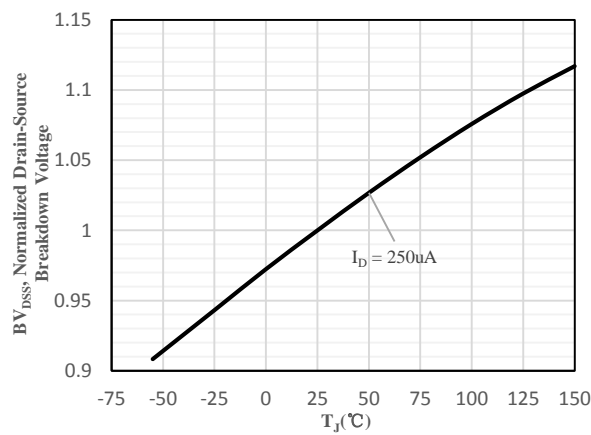


Fig 11 Normalized Breakdown Voltage vs. Junction Temperature

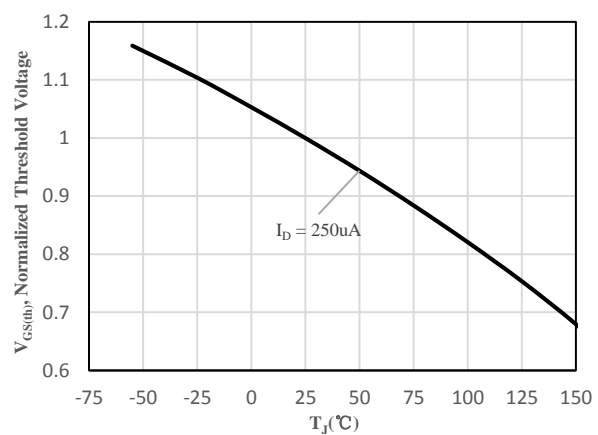


Fig 12 Normalized $V_{GS(th)}$ vs. Junction Temperature

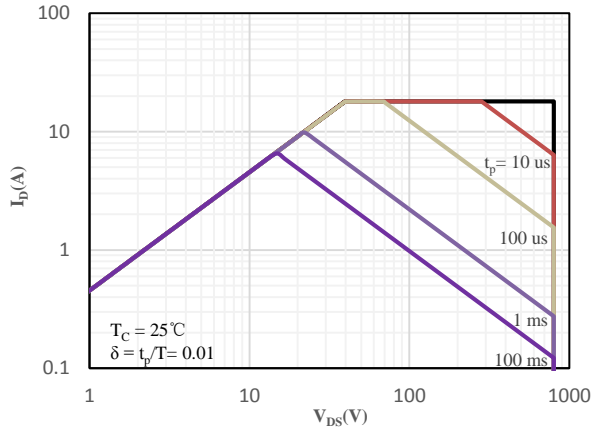


Fig 13 Safe Operating Area

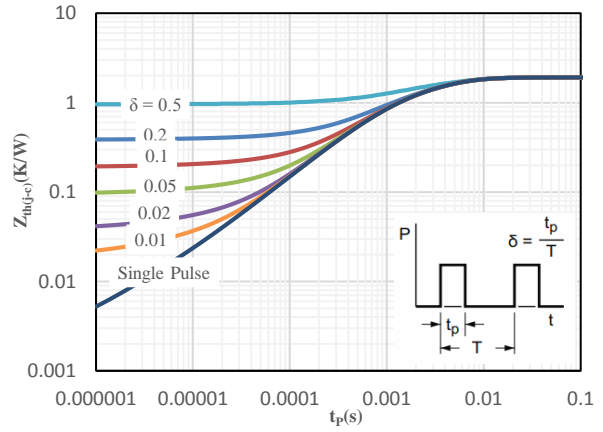
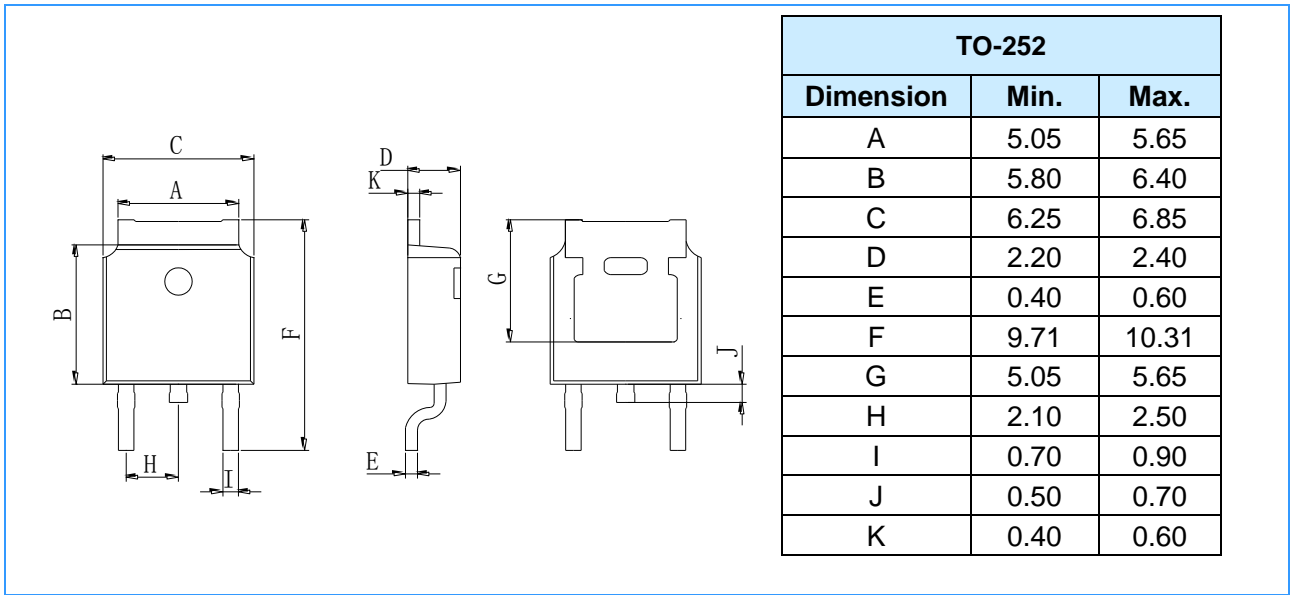


Fig 14 Maximum transient thermal impedance

Package Outline Dimensions (Unit: mm)



Mounting Pad Layout (Unit: mm)

