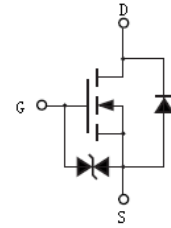


Features

- Low power loss by high speed switching and low on-resistance
- Excellent thermal behavior
- Very low FOM for fast switching efficiency
- Product validation acc. JEDEC Standard
- Integrated ESD protection diode: HBM: JESD22-A114-B: 2

HF

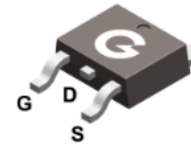


APPLICATIONS

- PFC power supply stages
- Lighting applications
- Adapter

Mechanical Data

- Case: TO-252
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte tin-plated leads; solderability-per MIL-STD-202, Method 208



TO-252

Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
SJM70R600D	TO-252	80 pcs / Tube & 2500 pcs / Tape & Reel	SJM70R600D

Maximum Ratings (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	700	V
Gate-to-Source Voltage (Static)	V_{GSS}	± 20	V
Continuous Drain Current ($T_C = 25^\circ\text{C}$)	I_D	8.5	A
Continuous Drain Current ($T_C = 100^\circ\text{C}$)		5.4	A
Pulsed Drain Current ($t_p = 10\mu\text{s}$, $T_C = 25^\circ\text{C}$)	I_{DM}	34	A
Single Pulse Avalanche Energy ^{*3}	E_{AS}	160	mJ
Power Dissipation ($T_C = 25^\circ\text{C}$)	P_D	90	W
Operating Junction Temperature Range	T_J	-55 ~ +150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	-	1	1.4	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Air ^{*1}	$R_{\theta JA}$	-	50	62	$^\circ\text{C/W}$

Electrical Characteristics (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
V_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	700	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 700V, V_{GS} = 0V$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 1	μA
On Characteristics						
$R_{DS(ON)}$	Drain-Source On-resistance ^{*2}	$V_{GS} = 10V, I_D = 3.5A$	-	0.53	0.6	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	V
R_G	Gate Resistance	$V_{GS} = 0V, f = 1MHz$	-	7.3	-	Ω
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V$	-	697	-	μF
C_{OSS}	Output Capacitance	$V_{DS} = 40V$	-	72	-	
C_{RSS}	Reverse Transfer Capacitance	$f = 250kHz$	-	1	-	
Switching Characteristics						
$t_{d(ON)}$	Turn-on Delay Time ^{*4}	$V_{DD} = 350V$	-	25	-	ns
t_r	Turn-on Rise Time [*]	$V_{GS} = 10V$	-	19	-	
$t_{d(OFF)}$	Turn-Off Delay Time ^{*4}	$R_G = 25\Omega$	-	87	-	
t_f	Turn-Off Fall Time ^{*4}	$I_D = 3.3A$	-	18	-	
Q_G	Total Gate-Charge	$V_{DD} = 560V$	-	19.2	-	nC
Q_{GS}	Gate to Source Charge	$V_{GS} = 10V$	-	2.6	-	
Q_{GD}	Gate to Drain (Miller) Charge	$I_D = 7A$	-	7.5	-	
Source-Drain Diode Characteristics						
V_{SD}	Diode Forward Voltage ^{*2}	$I_{SD} = 7A, V_{GS} = 0V$	-	0.9	1.4	V
t_{rr}	Reverse Recovery Time	$I_F = 2.5A, V_R = 400V$	-	225	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt = 100A/\mu s$	-	1.66	-	μC

Notes:

1. The data tested by surface mounted on a minimum recommended FR-4 board
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The E_{AS} data shows Max. rating. The test condition is $V_{DD} = 100V, V_{GS} = 15V, L = 50mH$
4. Guaranteed by design, not subject to production

Ratings and Characteristics Curves (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

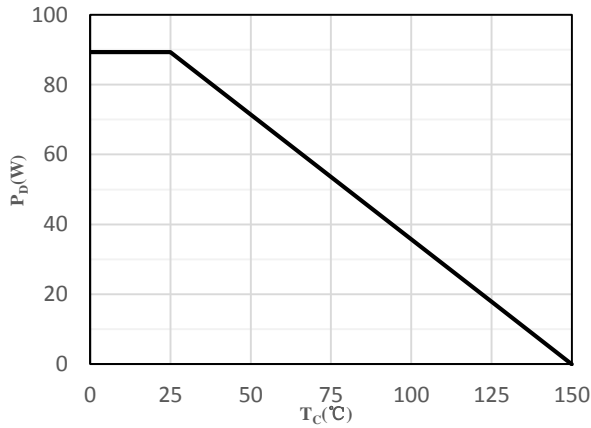


Fig 1 Power Dissipation

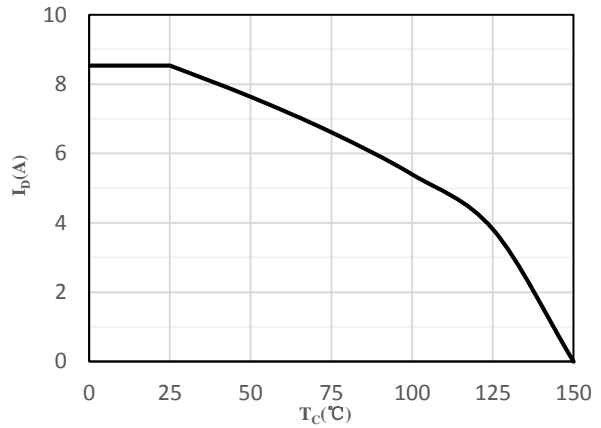


Fig 2 Drain Current

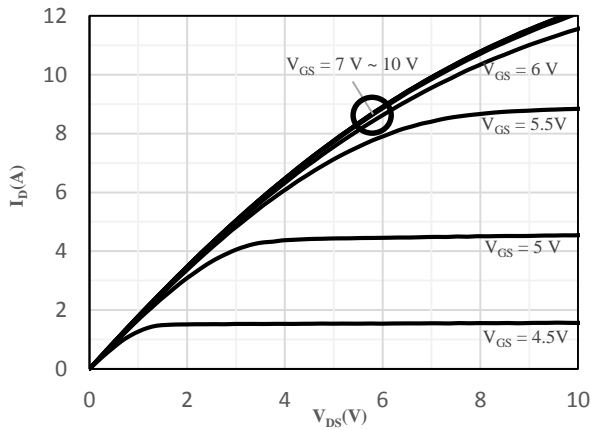


Fig 3 Typical Output Characteristics

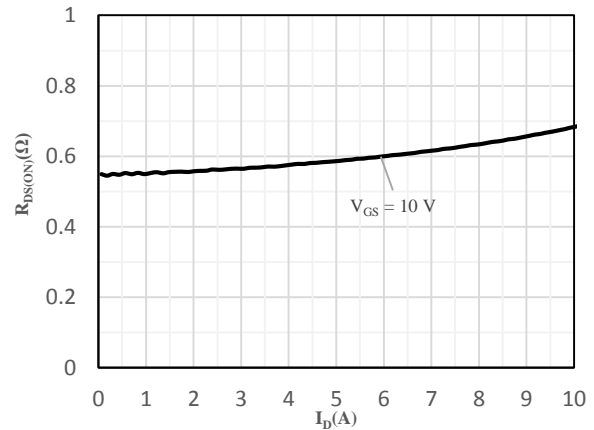


Fig 4 On-Resistance vs. Drain Current and Gate Voltage

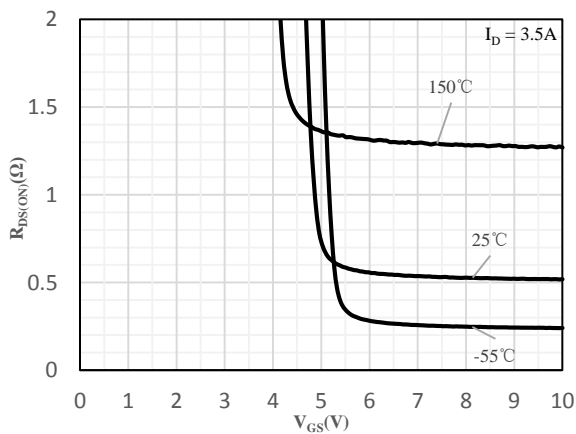


Fig 5 On-Resistance vs. Gate-Source Voltage

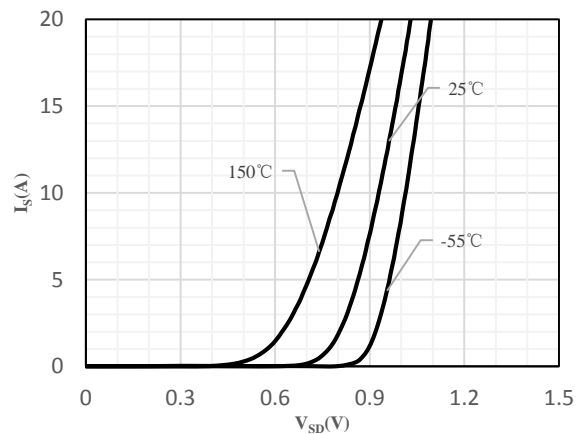


Fig 6 Body-Diode Characteristics

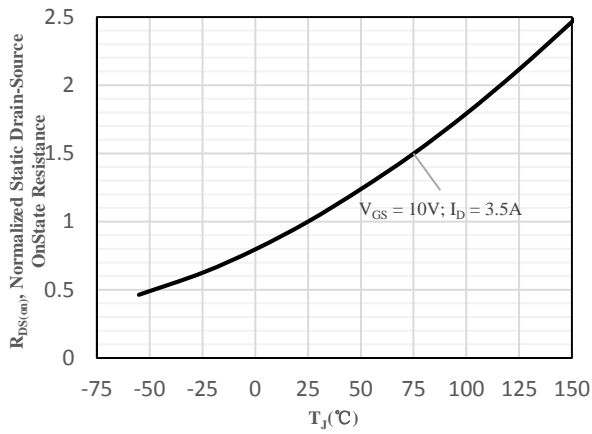


Fig 7 Normalized On-Resistance vs. Junction Temperature

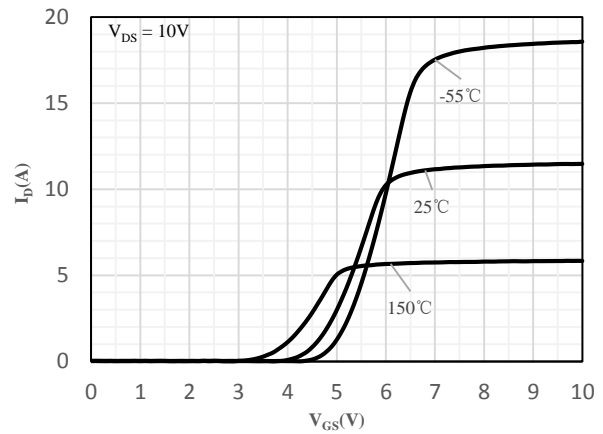


Fig 8 Transfer Characteristics

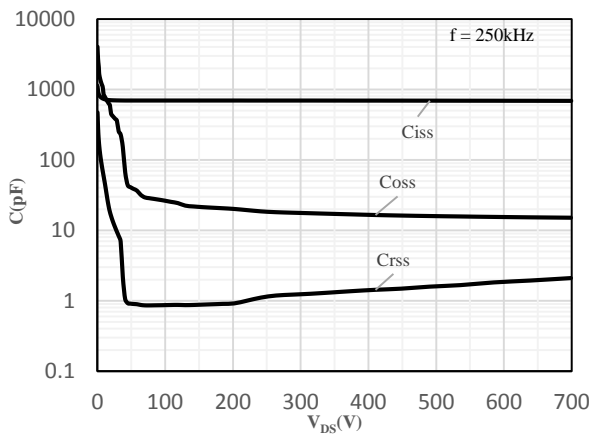


Fig 9 Capacitance Characteristics

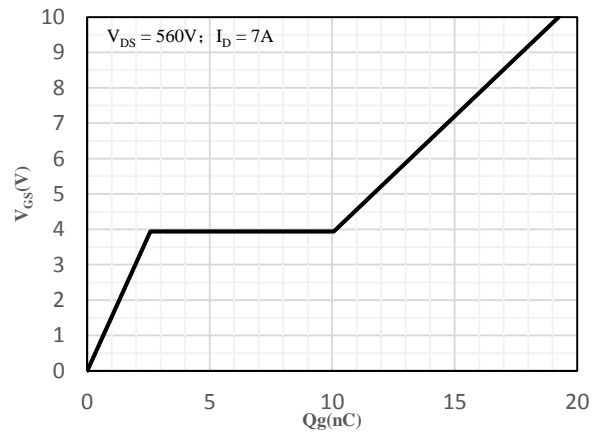


Fig 10 Gate-Charge Characteristics

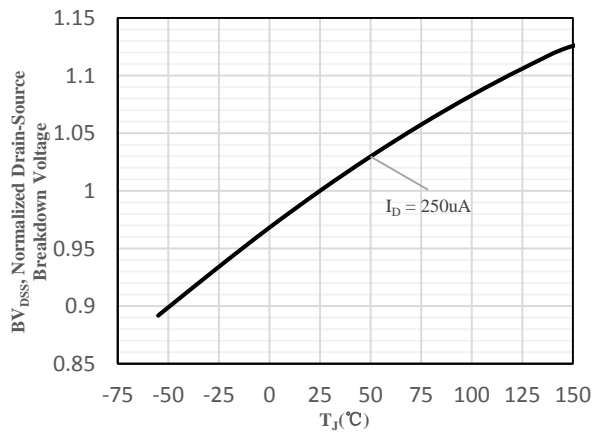


Fig 11 Normalized Breakdown Voltage vs. Junction Temperature

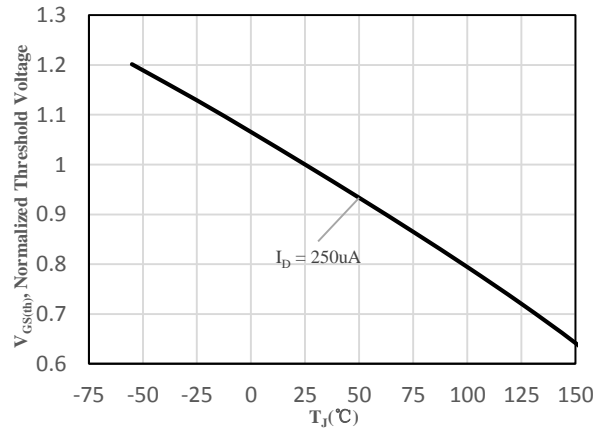


Fig 12 Normalized $V_{GS(th)}$ vs. Junction Temperature

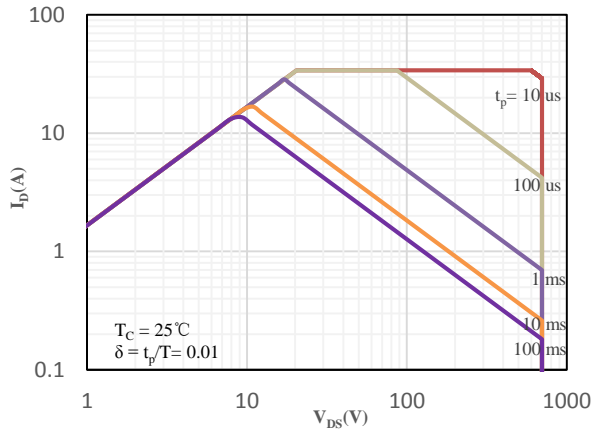


Fig 13 Safe Operation Area

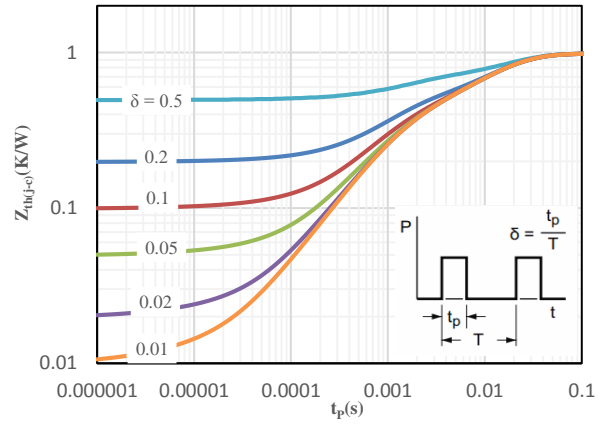
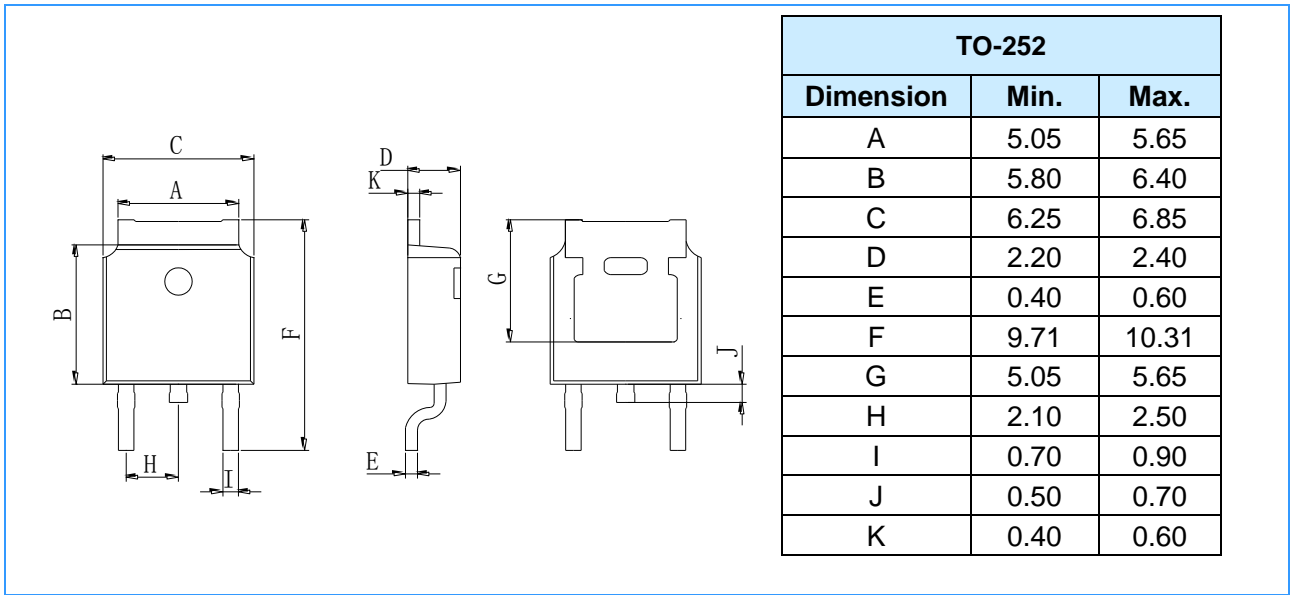
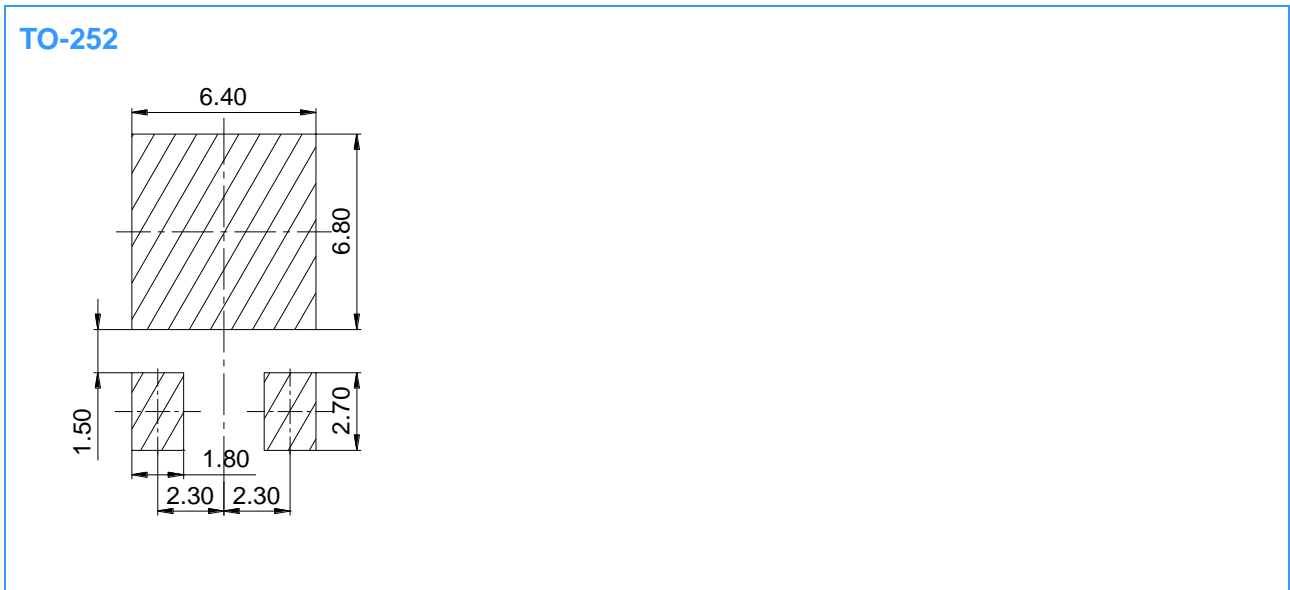


Fig 14 Maximum transient thermal impedance

Package Outline Dimensions (Unit: mm)



Mounting Pad Layout (Unit: mm)



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