

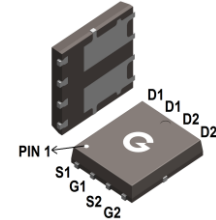
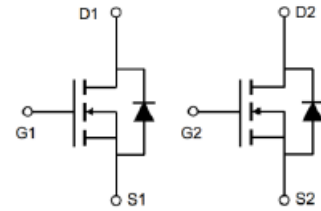
Features

- Super low gate charge
- Green device available
- Excellent C_{av} / d_t effect decline
- Advanced high cell density trench technology
- JESD22-A114-B ESD rating of class 1B per human body model

HF

Mechanical Data

- Case: PDFN5x6-8LC
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte tin-plated leads; solderability-per MIL-STD-202, Method 208



PDFN5x6-8LC

Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
GBLN6601-5DL8	PDFN5x6-8LC	5000 pcs / Tape & Reel	GBLN6601

Maximum Ratings (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	V
Gate-to-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current ($T_C = 25^\circ\text{C}$)	I_D	43	A
Continuous Drain Current ($T_C = 100^\circ\text{C}$)		30	A
Pulsed Drain Current ($t_p = 10\mu\text{s}$, $T_C = 25^\circ\text{C}$)	I_{DM}	215	A
Single Pulse Avalanche Energy ^{*3}	E_{AS}	40	mJ
Power Dissipation ($T_C = 25^\circ\text{C}$, $R_{\theta JC}$, bottom,)	P_D	83	W
Operating Junction Temperature Range	T_J	-55 ~ +175	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 ~ +175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance Junction-to-Case, top	$R_{\theta JC}$	-	-	4.5	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Case, bottom		-	1.45	1.8	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Air ^{*1}	$R_{\theta JA}$	-	-	100	$^\circ\text{C}/\text{W}$

Electrical Characteristics (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
V_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48V, V_{GS} = 0V$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 100	nA
On Characteristics						
$R_{DS(ON)}$	Drain-Source On-resistance ^{*2}	$V_{GS} = 10V, I_D = 20A$	-	15	20	m Ω
		$V_{GS} = 4.5V, I_D = 15A$	-	20	24	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.7	2.5	V
R_G	Gate Resistance	$V_{GS} = 0V, f = 1MHz$	-	2.8	-	Ω
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1.0MHz$	-	1659	-	pF
C_{OSS}	Output Capacitance		-	158	-	
C_{RSS}	Reverse Transfer Capacitance		-	132	-	
Switching Characteristics						
$t_{d(ON)}$	Turn-on Delay Time ^{*4}	$V_{DD} = 30V$ $V_{GS} = 10V$ $R_G = 3\Omega$ $I_D = 15A$	-	7.4	-	ns
t_r	Turn-on Rise Time ^{*4}		-	5.1	-	
$t_{d(OFF)}$	Turn-Off Delay Time ^{*4}		-	28.3	-	
t_f	Turn-Off Fall Time ^{*4}		-	5.5	-	
Q_G	Total Gate-Charge	$V_{DD} = 48V$ $V_{GS} = 10V$ $I_D = 15A$	-	37	-	nC
Q_{GS}	Gate to Source Charge		-	5	-	
Q_{GD}	Gate to Drain (Miller) Charge		-	10.7	-	
Source-Drain Diode Characteristics						
V_{SD}	Diode Forward Voltage ^{*2}	$I_{SD} = 5A, V_{GS} = 0V, T_J = 25^\circ\text{C}$	-	0.79	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V, I_F = 15A$ $di/dt = 100A/\mu s$	-	30	-	ns
Q_{rr}	Reverse Recovery Charge		-	25	-	nC

Notes:

1. The data tested by surface mounted on a minimum recommended FR-4 board
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The E_{AS} data shows Max. rating. The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.1mH$
4. Guaranteed by design, not subject to production

Ratings and Characteristics Curves (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

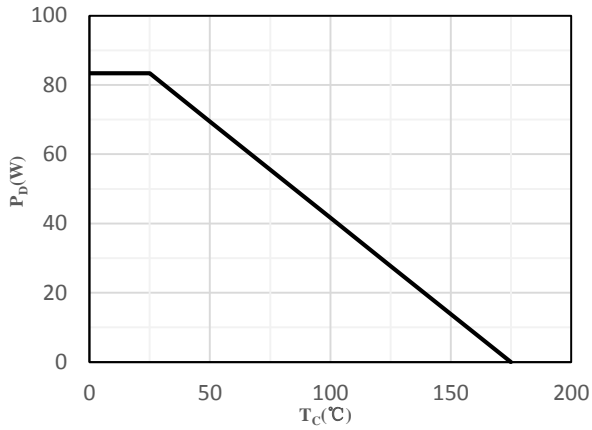


Fig 1 Power Dissipation

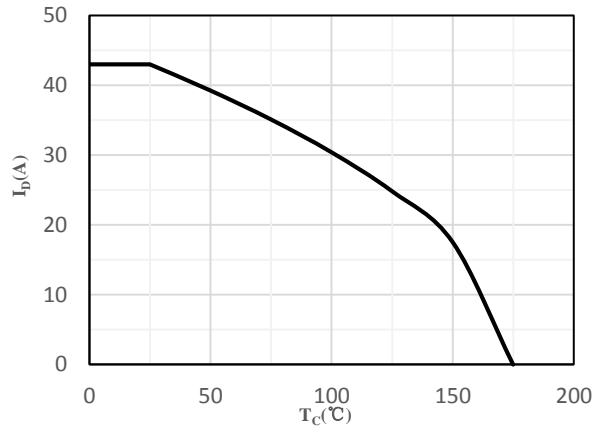


Fig 2 Drain Current

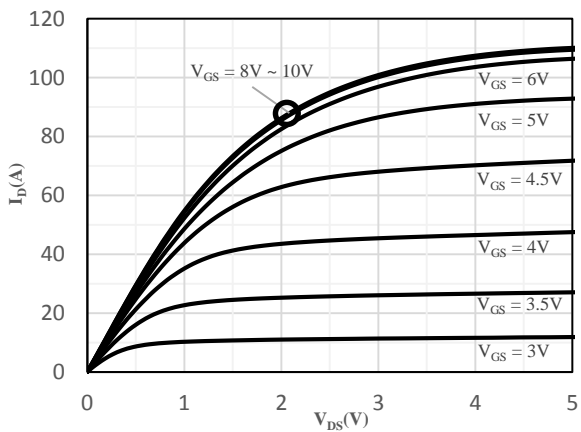


Fig 3 Typical Output Characteristics

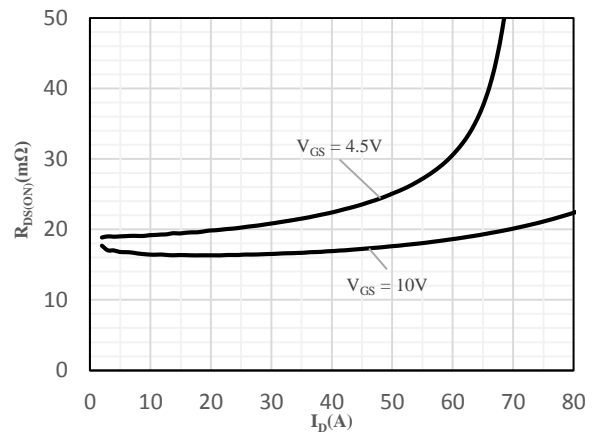


Fig 4 On-Resistance vs. Drain Current and Gate Voltage

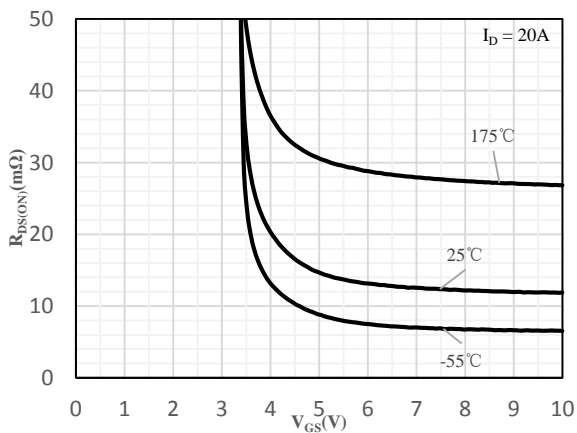


Fig 5 On-Resistance vs. Gate-Source Voltage

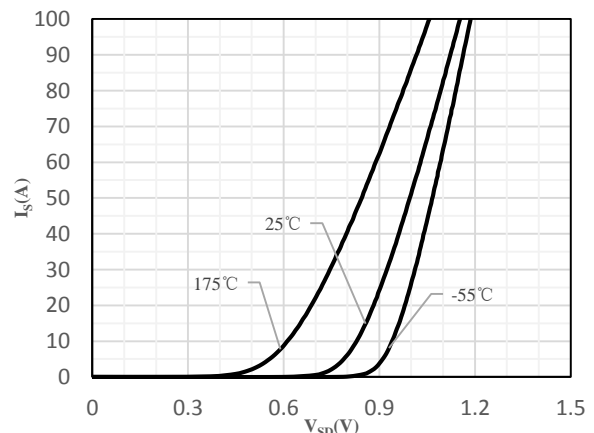


Fig 6 Body-Diode Characteristics

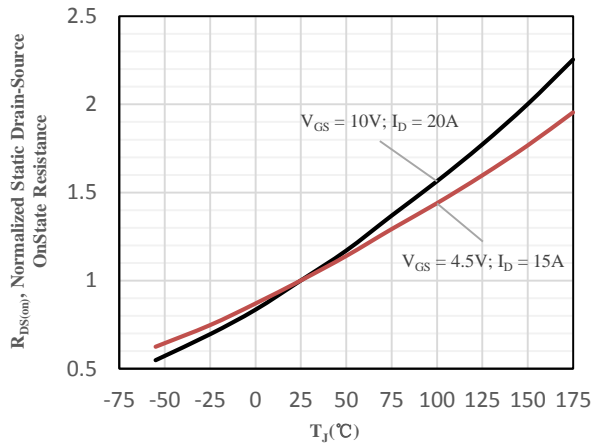


Fig 7 Normalized On-Resistance vs. Junction Temperature

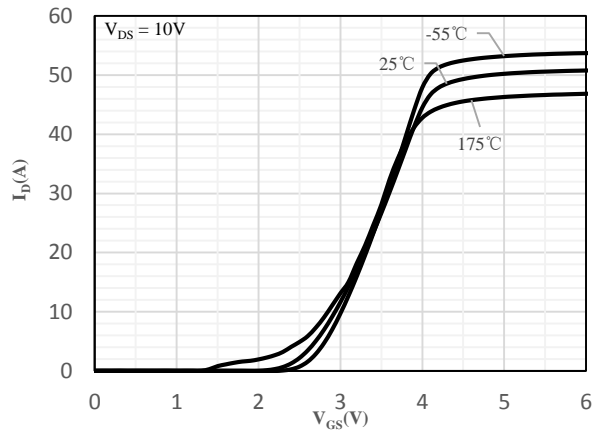


Fig 8 Transfer Characteristics

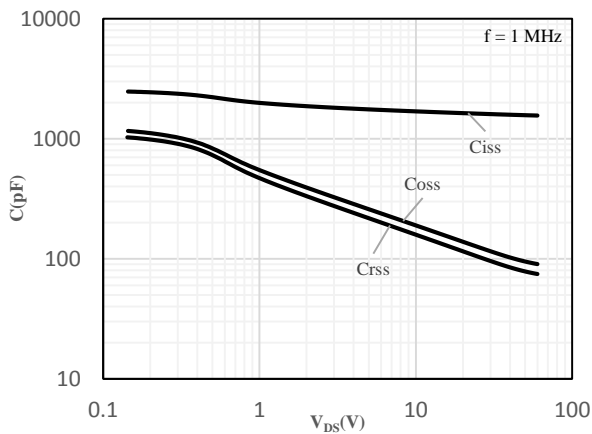


Fig 9 Capacitance Characteristics

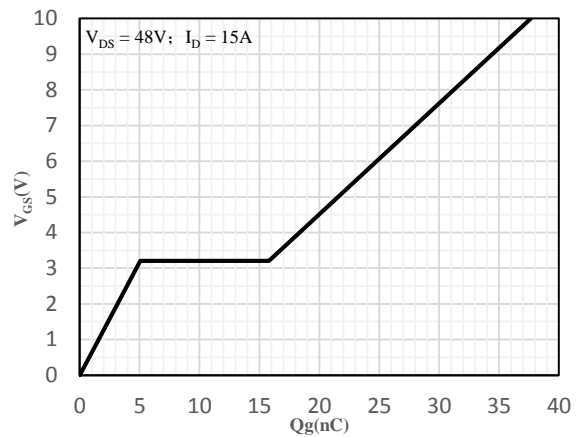


Fig 10 Gate-Charge Characteristics

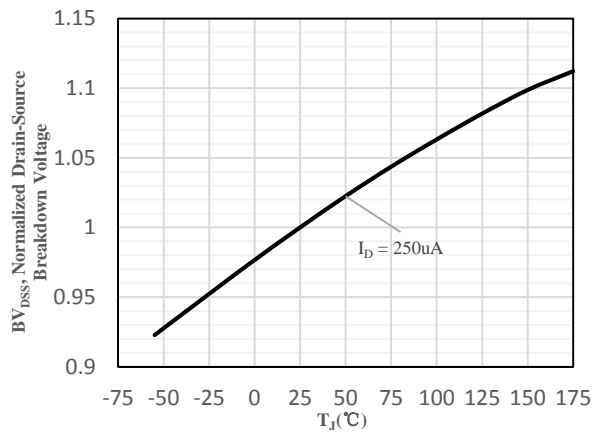


Fig 11 Normalized Breakdown Voltage vs. Junction Temperature

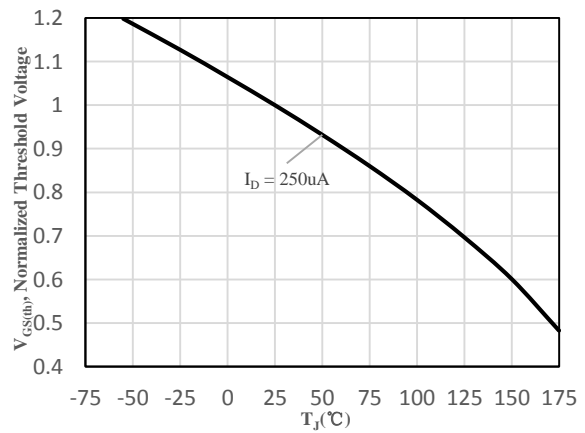


Fig 12 Normalized $V_{GS(th)}$ vs. Junction Temperature

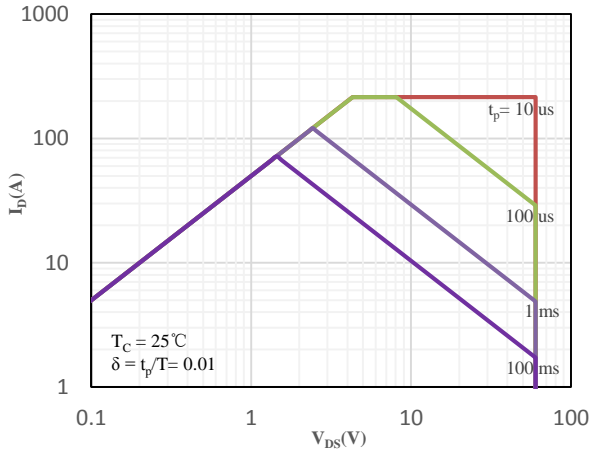


Fig 13 Safe Operation Area

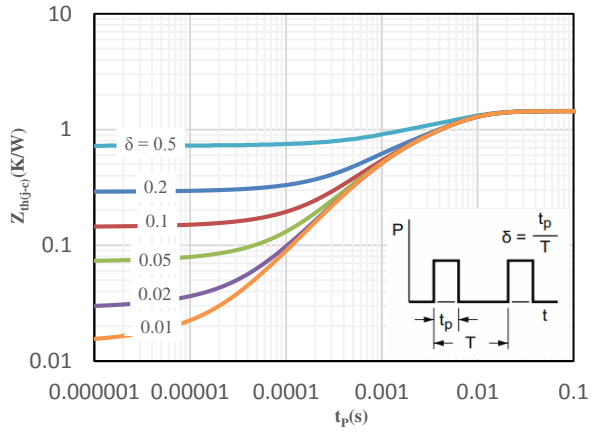
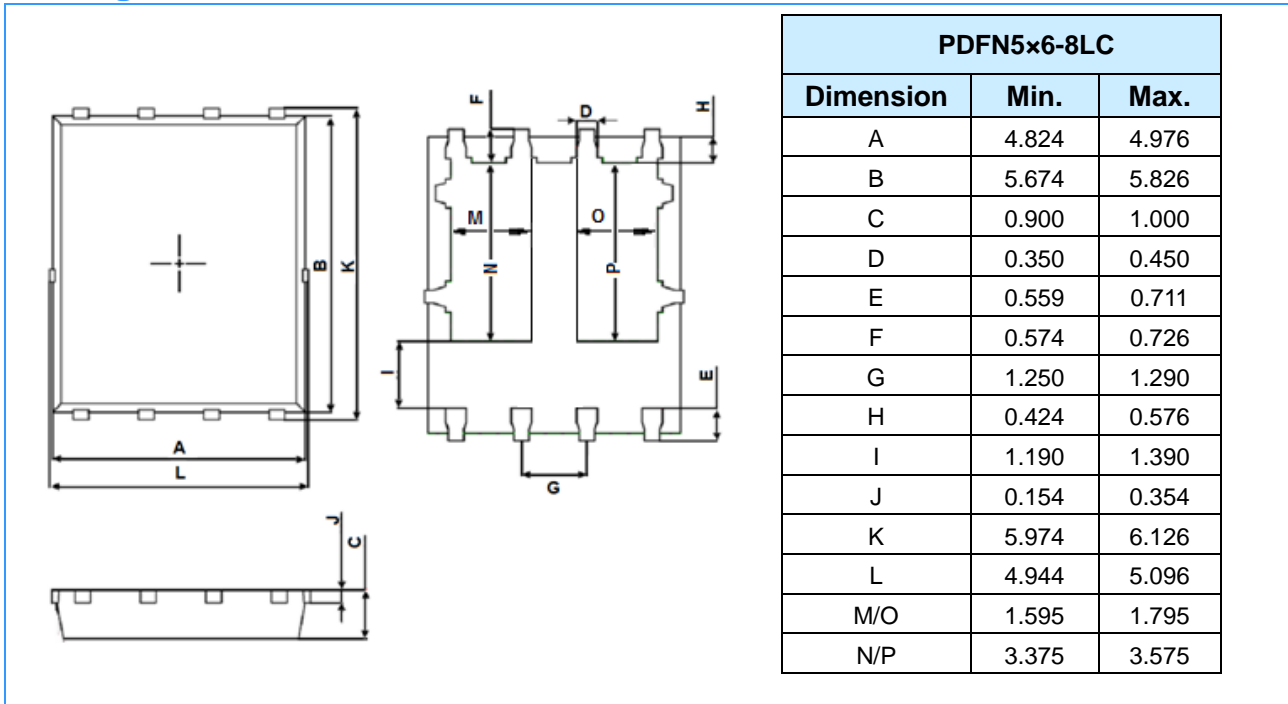
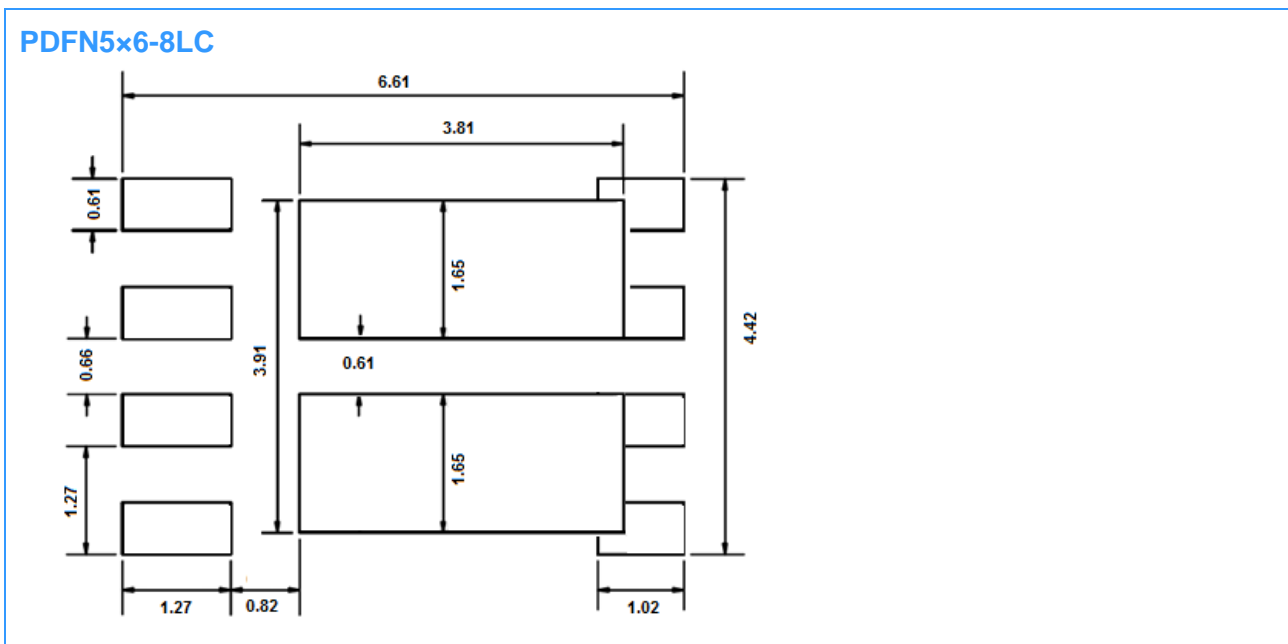


Fig 14 Maximum transient thermal impedance

Package Outline Dimensions (Unit: mm)



Mounting Pad Layout (Unit: mm)



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